Dual 350 MHz Low Power Amplifier

AD8012

FEATURES

Low Power
- 1.7 mA/Amplifier Supply Current
- Fully Specified for ±5 V and +5 V Supplies

High Output Current, 125 mA

High Speed
- 350 MHz, –3 dB Bandwidth (G = +1)
- 150 MHz, –3 dB Bandwidth (G = +2)
- 2,250 V/μs Slew Rate
- 20 ns Settling Time to 0.1%

Low Distortion
- –72 dBc Worst Harmonic @ 500 kHz, R_L = 100 Ω
- –66 dBc Worst Harmonic @ 5 MHz, R_L = 1 kΩ

Good Video Specifications (R_L = 1 kΩ, G = +2)
- 0.02% Differential Gain Error
- 0.06° Differential Phase Error
- Gain Flatness 0.1 dB to 40 MHz
- 60 ns Overdrive Recovery

Low Offset Voltage, 1.5 mV

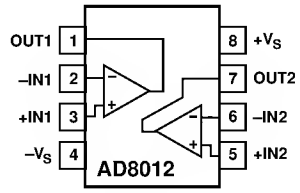
Low Voltage Noise, 2.5 nV/√Hz

Available in 8-Lead SOIC, and 8-Lead microSOIC

APPLICATIONS

XDSL, HDSL Line Driver
ADC Buffer
Professional Cameras
CCD Imaging System
Ultrasound Equipment
Digital Camera

FUNCTIONAL BLOCK DIAGRAM



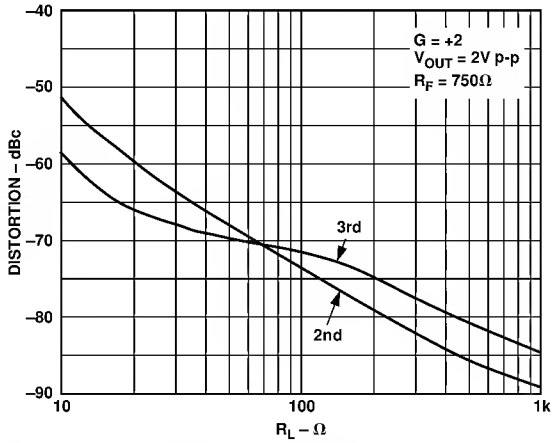


Figure 1. Distortion vs. Load Resistance, V_S = ±5 V, Frequency = 500 kHz

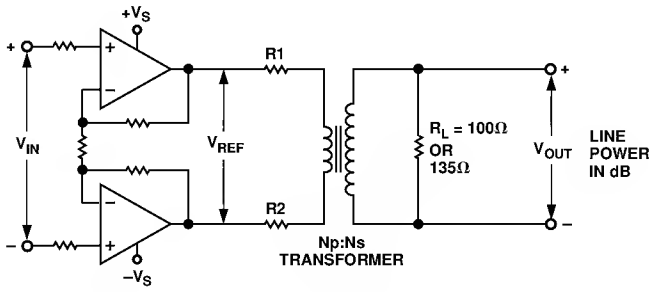


Figure 2. Differential Drive Circuit for XDSL Applications

PRODUCT DESCRIPTION

The AD8012 is a dual low power current feedback amplifier capable of providing 350 MHz bandwidth while using only 1.7 mA per amplifier. It is intended for use in high frequency, wide dynamic range systems where low distortion, high speed are essential and low power is critical.

With only 1.7 mA of supply current, the AD8012 also offers exceptional ac specs such as 20 ns settling time and 2,250 V/μs slew rate. The video specifications are 0.02% differential gain and 0.06 degree differential phase, excellent for such a low power amplifier. In addition, the AD8012 has a low offset of 1.5 mV.

The AD8012 is well suited for any application that requires high performance with minimal power.

The product is available in standard 8-lead SOIC or micro-SOIC packages and operates over the industrial temperature range –40°C to +85°C.

REV. 0

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AD8012- SPECIFICATIONS

DUAL SUPPLY (@ T_A = +25°C, V_S = ±5 V, G = +2, R_L = 100 Ω, R_F = R_G = 750 Ω, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, V_{OUT} < 0.4 V p-p, R_L = 1 kΩ	270	350		MHz
	G = +2, V_{OUT} < 0.4 V p-p, R_L = 1 kΩ	95	150		MHz
	G = +2, V_{OUT} < 0.4 V p-p, R_L = 100 Ω		90		MHz
0.1 dB Bandwidth	V_{OUT} < 0.4 V p-p, R_L = 1 kΩ/100 Ω		40/23		MHz
Large Signal Bandwidth	V_{OUT} = 4 V p-p		75		MHz
Slew Rate	V_{OUT} = 4 V p-p		2,250		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p		3		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		20		ns
	0.02%, V_{OUT} = 2 V p-p		35		ns
Overdrive Recovery	2× Overdrive		60		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p, G = +2				
2nd Harmonic	500 kHz, R_L = 1 kΩ/100 Ω		–89/–73		dBc
	5 MHz, R_L = 1 kΩ/100 Ω		–78/–62		dBc
3rd Harmonic	500 kHz, R_L = 1 kΩ/100 Ω		–84/–72		dBc
	5 MHz, R_L = 1 kΩ/100 Ω		–66/–52		dBc
Output IP3	500 kHz, Δf = 10 kHz, R_L = 1 kΩ/100 Ω		30/40		dBm
IMD	500 kHz, Δf = 10 kHz, R_L = 1 kΩ/100 Ω		–79/–77		dBc
Crosstalk	5 MHz, R_L = 100 Ω		–70		dB
Input Voltage Noise	f = 10 kHz		2.5		nV/√Hz
Input Current Noise	f = 10 kHz, +Input, –Input		15		pA/√Hz
Differential Gain	f = 3.58 MHz, R_L = 150 Ω/1 kΩ, G = +2		0.02/0.02		%
Differential Phase	f = 3.58 MHz, R_L = 150 Ω/1 kΩ, G = +2		0.3/0.06		Degrees
DC PERFORMANCE					
Input Offset Voltage			±1.5	±4	mV
	T_{MIN}–T_{MAX}			±5	mV
Open-Loop Transimpedance	V_{OUT} = ±2 V, R_L = 100 Ω	240	500		kΩ
	T_{MIN}–T_{MAX}	200			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		450		kΩ
Input Capacitance	+Input		2.3		pF
Input Bias Current	+Input, –Input		±3	±12	µA
	+Input, –Input, T_{MIN}–T_{MAX}			±15	µA
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	–56	–60		dB
Input Common-Mode Voltage Range		±3.8	±4.1		V
OUTPUT CHARACTERISTICS					
Output Resistance	G = +2		0.1		Ω
Output Voltage Swing		±3.85	±4		V
Output Current	T_{MIN}–T_{MAX}	70	125		mA
Short Circuit Current			500		mA
POWER SUPPLY					
Supply Current/Amp			1.7	1.8	mA
	T_{MIN}–T_{MAX}			1.9	mA
Operating Range	Dual Supply	±1.5		±6.0	V
Power Supply Rejection Ratio		–58	–60		dB

Specifications subject to change without notice.

SINGLE SUPPLY (@ T_A +25°C, V_S = +5 V, G = +2, R_L = 100 Ω, R_F = R_G = 750 Ω, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, V_{OUT} < 0.4 V p-p, R_L = 1 kΩ	220	300		MHz
	G = +2, V_{OUT} < 0.4 V p-p, R_L = 1 kΩ	90	140		MHz
	G = +2, V_{OUT} < 0.4 V p-p, R_L = 100 Ω		85		MHz
0.1 dB Bandwidth	V_{OUT} < 0.4 V p-p, R_L = 1 kΩ/100 Ω		43/24		MHz
Large Signal Bandwidth	V_{OUT} = 2 V p-p		60		MHz
Slew Rate	V_{OUT} = 3 V p-p		1,200		V/µs
Rise and Fall Time	V_{OUT} = 2 V p-p		2		ns
Settling Time	0.1%, V_{OUT} = 2 V p-p		25		ns
	0.02%, V_{OUT} = 2 V p-p		40		ns
Overdrive Recovery	2× Overdrive		60		ns
NOISE/HARMONIC PERFORMANCE					
Distortion	V_{OUT} = 2 V p-p, G = +2				
2nd Harmonic	500 kHz, R_L = 1 kΩ/100 Ω		–87/–71		dBc
	5 MHz, R_L = 1 kΩ/100 Ω		–77/–61		dBc
3rd Harmonic	500 kHz, R_L = 1 kΩ/100 Ω		–89/–72		dBc
	5 MHz, R_L = 1 kΩ/100 Ω		–78/–52		dBc
Output IP3	500 kHz, R_L = 1 kΩ/100 Ω		30/40		dBm
IMD	500 kHz, R_L = 1 kΩ/100 Ω		–77/–80		dBc
Crosstalk	5 MHz, R_L = 100 Ω		–70		dB
Input Voltage Noise	f = 10 kHz		2.5		nV/√Hz
Input Current Noise	f = 10 kHz, +Input, –Input		15		pA/√Hz
	Black Level Clamped to +2 V, f = 3.58 MHz				
Differential Gain	R_L = 150 Ω/1 kΩ		0.03/0.03		%
Differential Phase	R_L = 150 Ω/1 kΩ		0.4/0.08		Degrees
DC PERFORMANCE					
Input Offset Voltage			±1	±3	mV
	T_{MIN}–T_{MAX}			±4	mV
Open-Loop Transimpedance	V_{OUT} = 2 V p-p, R_L = 100 Ω	200	400		kΩ
	T_{MIN}–T_{MAX}	150			kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		450		kΩ
Input Capacitance	+Input		2.3		pF
Input Bias Current	+Input, –Input		±3	±12	µA
	+Input, –Input, T_{MIN}–T_{MAX}			±15	µA
Common-Mode Rejection Ratio	V_{CM} = 1.5 V to 3.5 V	–56	–60		dB
Input Common-Mode Voltage Range		1.5 to 3.5	1.2 to 3.8		V
OUTPUT CHARACTERISTICS					
Output Resistance	G = +2		0.1		Ω
Output Voltage Swing		1 to 4	0.9 to 4.2		V
Output Current	T_{MIN}–T_{MAX}	50	100		mA
Short Circuit Current			500		mA
POWER SUPPLY					
Supply Current/Amp			1.55	1.75	mA
	T_{MIN}–T_{MAX}			1.85	mA
Operating Range	Single Supply	3		12	V
Power Supply Rejection Ratio		–58	–60		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ..... 12.6 V
Internal Power Dissipation[2]
Small Outline Package (R) ..... 0.8 W
microSOIC Package (RM) ..... 0.6 W
Input Voltage (Common Mode) ..... $\pm V_S$
Differential Input Voltage ..... ±2.5 V
Output Short Circuit Duration
..... Observe Power Derating Curves
Storage Temperature Range RM, R ..... –65°C to +125°C
Operating Temperature Range (A Grade) .. –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air at +25°C
8-Lead SOIC Package: θ_{JA} = 160°C/Watt
8-Lead microSOIC Package: θ_{JA} = 200°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options
AD8012AR	–40°C to +85°C	8-Lead SOIC	SO-8
AD8012ARM	–40°C to +85°C	8-Lead microSOIC	RM-08

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8012 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

The output stage of the AD8012 is designed for maximum load current capability. As a result, shorting the output to common can cause the AD8012 to source or sink 500 mA. To ensure proper operation, it is necessary to observe the maximum power derating curves. Direct connection of the output to either power supply rail can destroy the device.

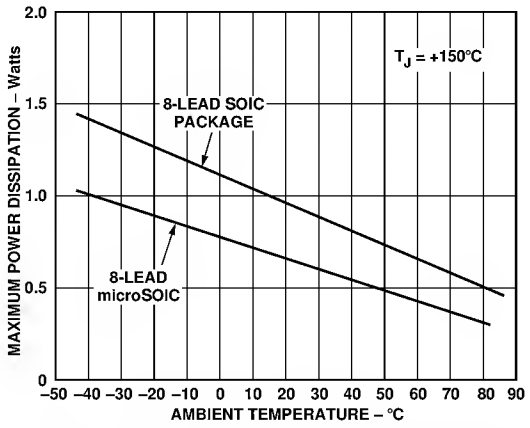


Figure 3. Plot of Maximum Power Dissipation vs. Temperature for AD8012

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8012 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

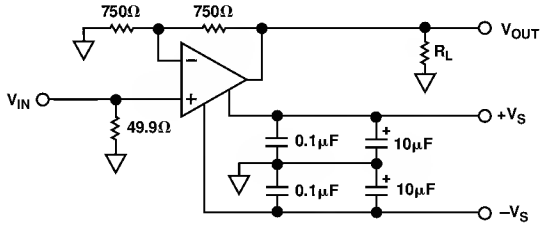


Figure 4. Test Circuit; Gain = +2

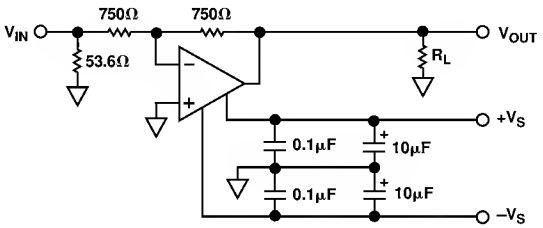


Figure 7. Test Circuit; Gain = –1

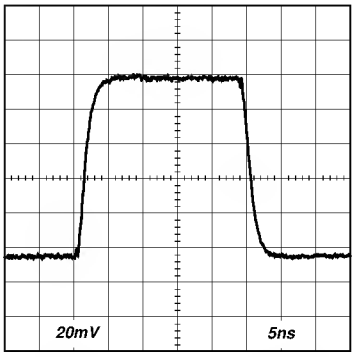


Figure 5. 100 mV Step Response; G = +2, V_S = ±2.5 V or ±5 V, R_L = 1 kΩ*

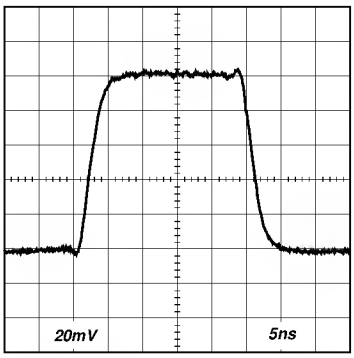


Figure 8. 100 mV Step Response; G = –1, V_S = ±2.5 V or ±5 V, R_L = 1 kΩ*

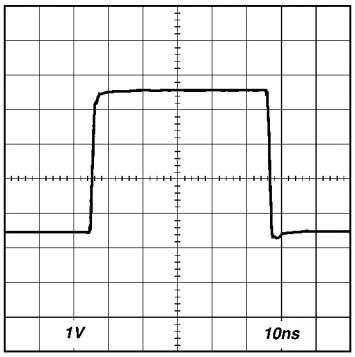


Figure 6. 4 V Step Response; G = +2, V_S = ±5 V, R_L = 1 kΩ

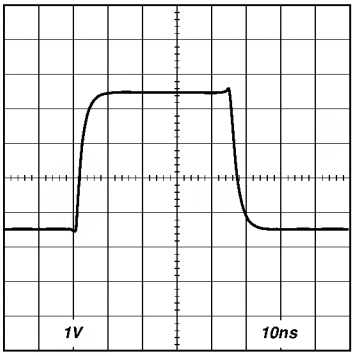


Figure 9. 4 V Step Response; G = –1, V_S = ±5 V, R_L = 1 kΩ

*NOTE: V_S = ±2.5 V operation is identical to V_S = +5 V single supply operation.

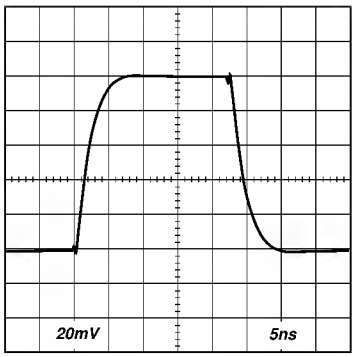


Figure 10. 100 mV Step Response; G = +2, V_S = ±2.5 V or ±5 V, R_L = 100 Ω*

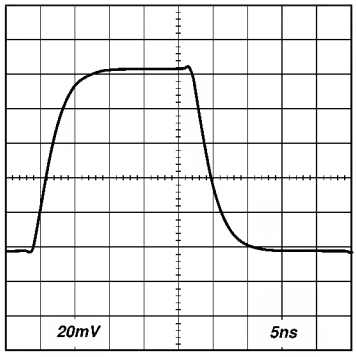


Figure 13. 100 mV Step Response; G = –1, V_S = ±2.5 V or ±5 V, R_L = 100 Ω*

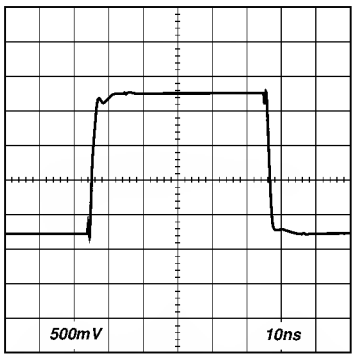


Figure 11. 2 V Step Response; G = +2, V_S = ±2.5 V, R_L = 100 Ω

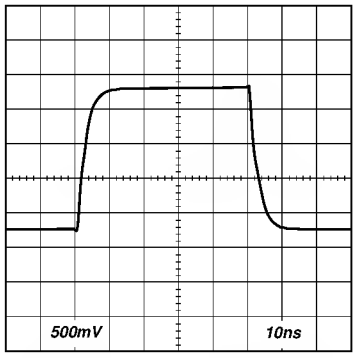


Figure 14. 2 V Step Response; G = –1, V_S = ±2.5 V, R_L = 100 Ω

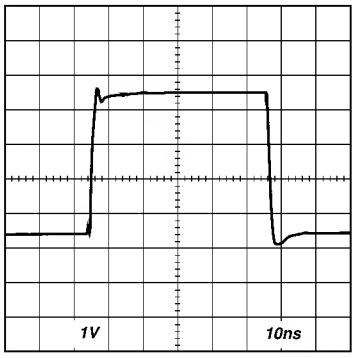


Figure 12. 4 V Step Response; G = +2, V_S = ±5 V, R_L = 100 Ω

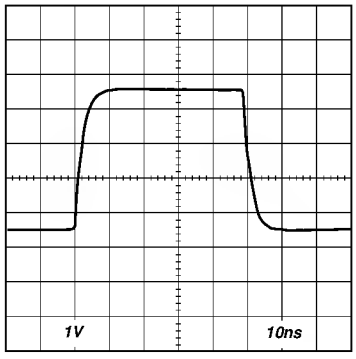


Figure 15. 4 V Step Response; G = –1, V_S = ±5 V, R_L = 100 Ω

*NOTE: V_S = ±2.5 V operation is identical to V_S = +5 V single supply operation.

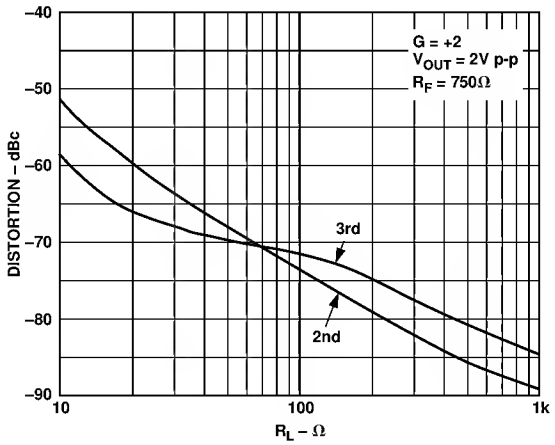


Figure 16. Distortion vs. Load Resistance; V_S =±5 V, Frequency =500 kHz

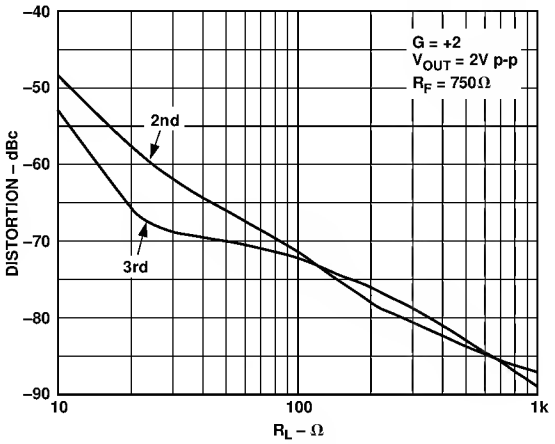


Figure 19. Distortion vs. Load Resistance; V_S =+5 V, Frequency = 500 kHz

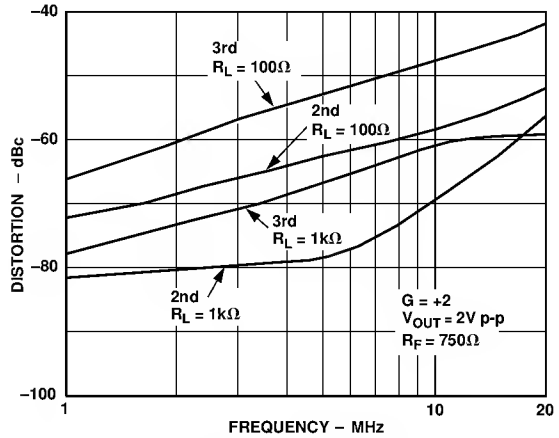


Figure 17. Distortion vs. Frequency; V_S =±5 V

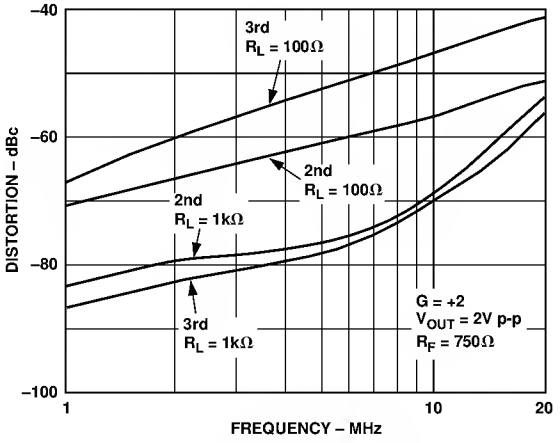


Figure 20. Distortion vs. Frequency; V_S =+5 V

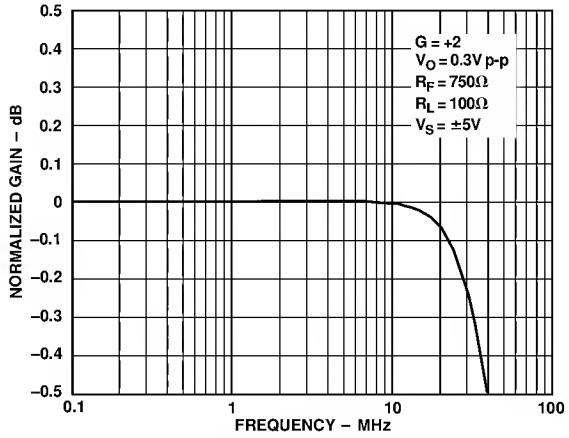


Figure 18. Gain Flatness; V_S =±5 V

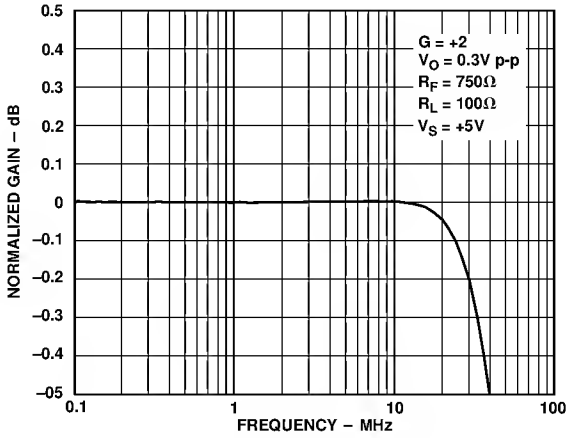


Figure 21. Gain Flatness; V_S =+5 V

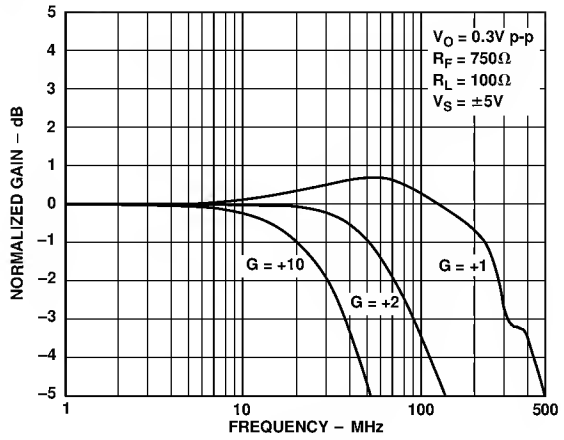


Figure 22. Frequency Response; V_S = ±5 V

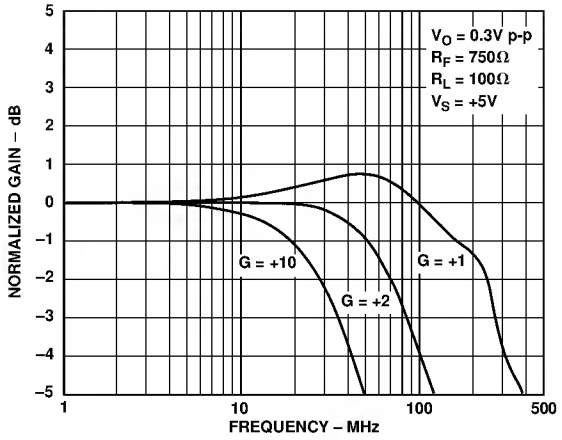


Figure 25. Frequency Response; V_S = +5 V

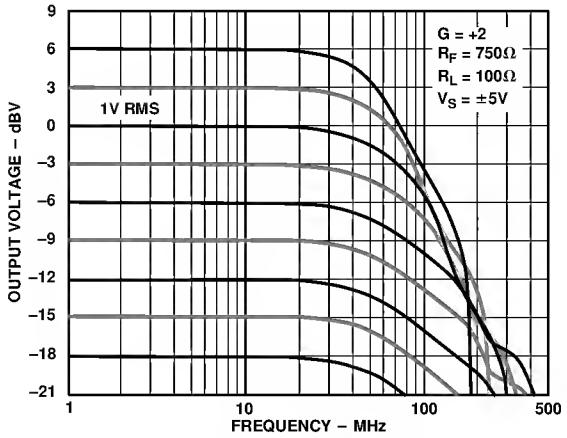


Figure 23. Output Voltage vs. Frequency; V_S = ±5 V, G = +2 V, R_L = 100 Ω

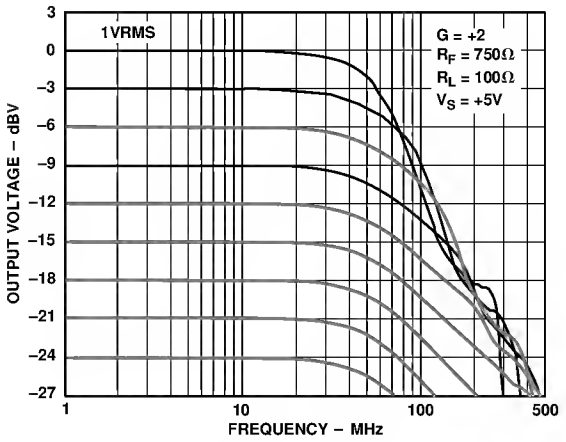


Figure 26. Output Voltage vs. Frequency; V_S = +5 V, G = +2 V, R_L = 100 Ω

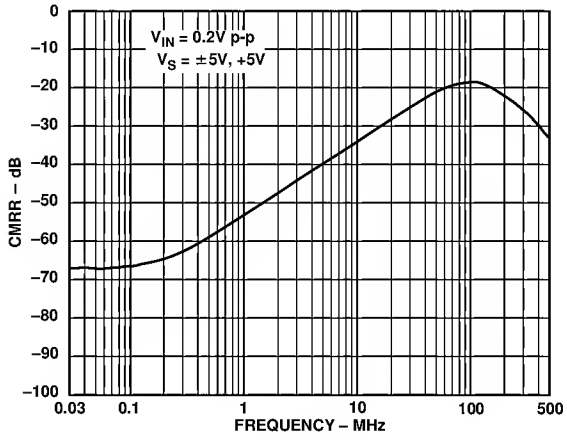


Figure 24. CMRR vs. Frequency; V_S = ±5 V, +5 V

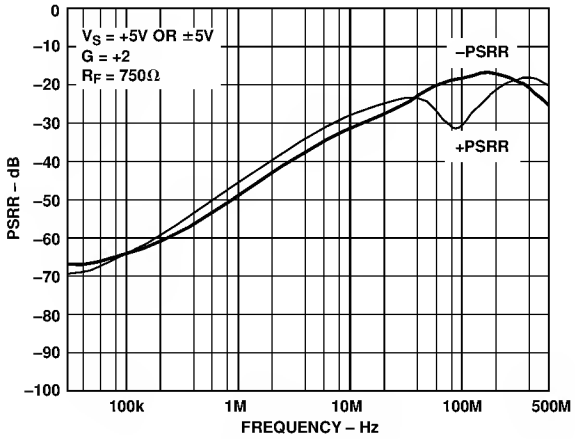


Figure 27. PSRR vs. Frequency; V_S = ±5 V, +5 V

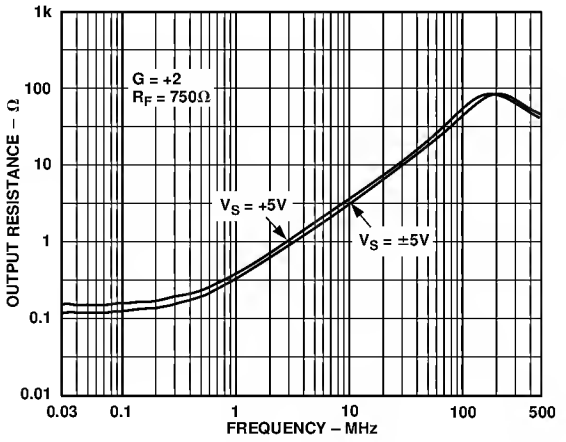


Figure 28. Output Resistance vs. Frequency

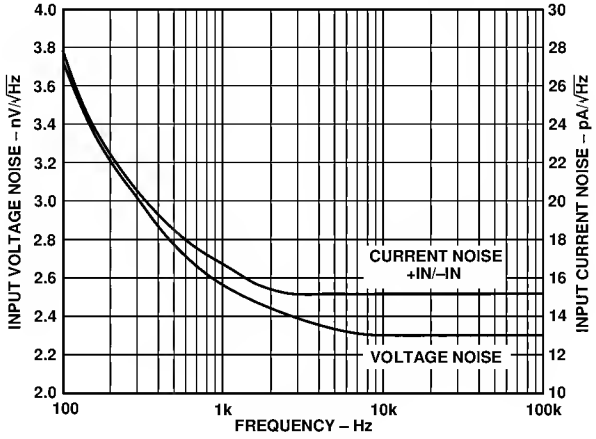


Figure 31. Noise vs. Frequency

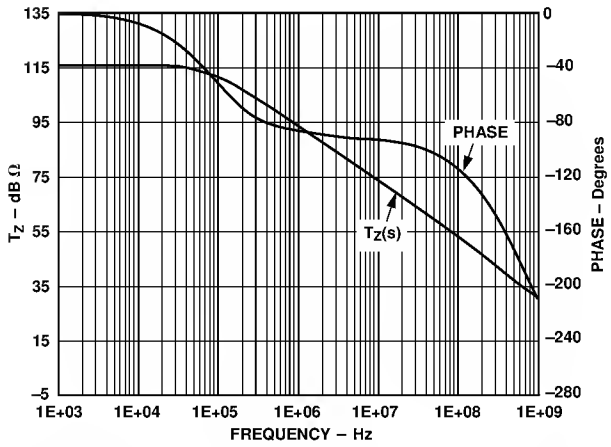


Figure 29. Open-Loop Transimpedance and Phase vs. Frequency

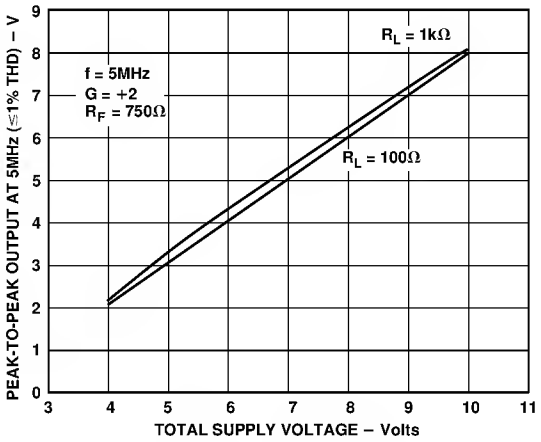


Figure 32. Output Swing vs. Supply

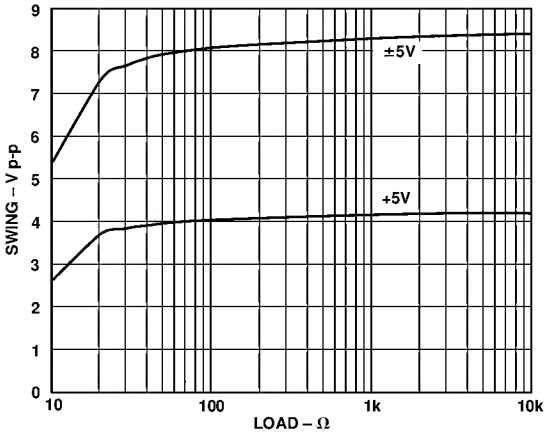


Figure 30. Output Swing vs. Load

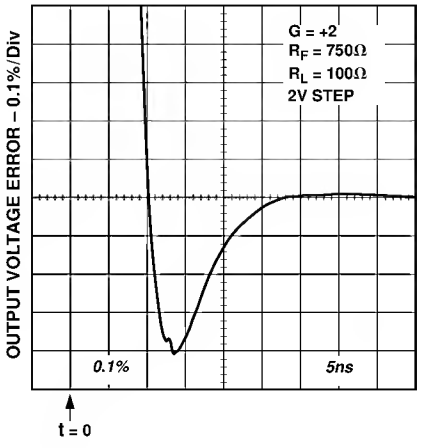


Figure 33. Settling Time, V_S =±5 V

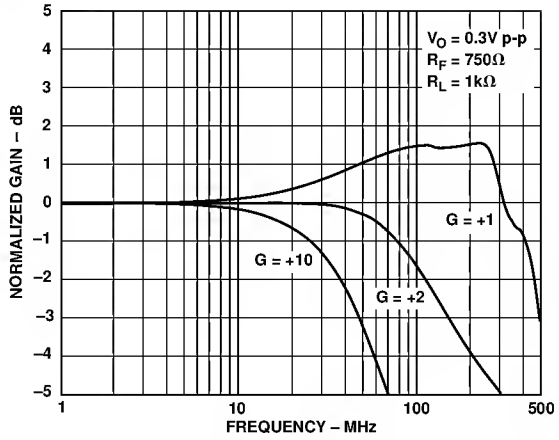


Figure 34. Frequency Response; V_S = ±5 V

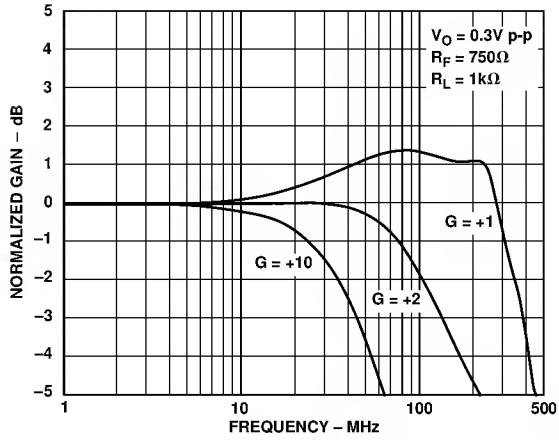


Figure 37. Frequency Response; V_S = +5 V

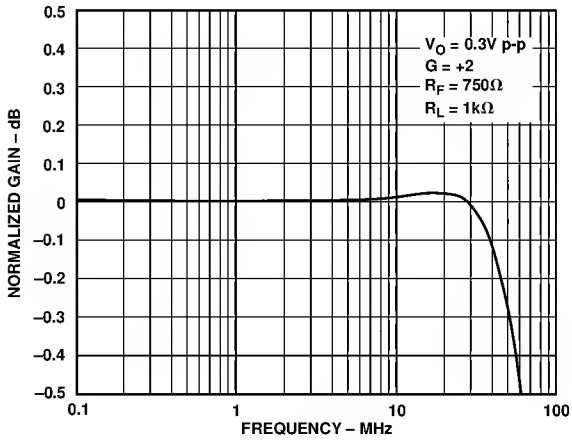


Figure 35. Gain Flatness; V_S = ±5 V

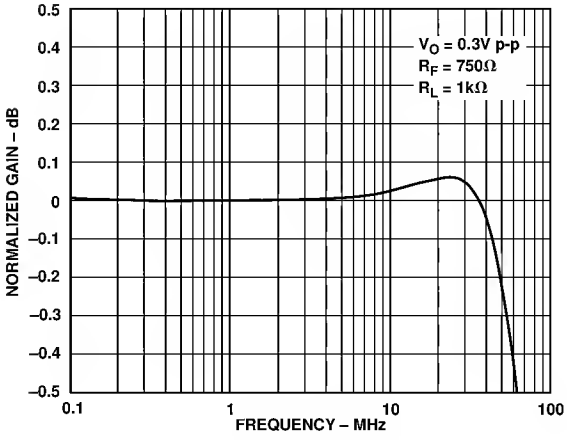


Figure 38. Gain Flatness; V_S = +5 V

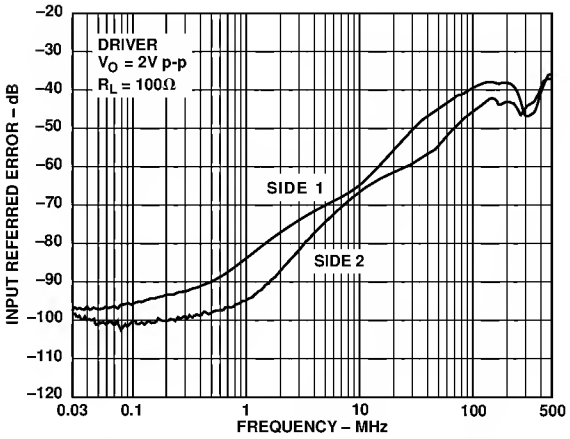


Figure 36. Crosstalk vs. Frequency

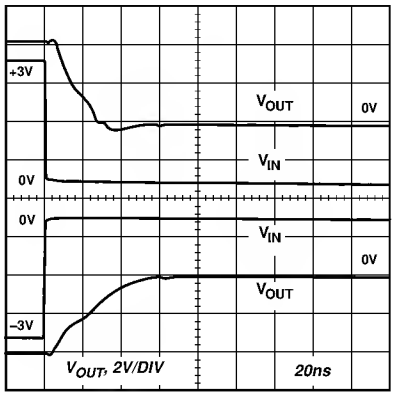


Figure 39. Overdrive Recovery; V_S = ±5 V, G = +2, R_F = 750 Ω, R_L = 100 Ω, V_{IN} = 3 V p-p (T = 1 µs)

THEORY OF OPERATION

The AD8012 is a dual high speed CF amplifier that attains new levels of bandwidth (BW), power, distortion and signal swing capability. Its wide dynamic performance (including noise) is the result of both a new complementary high speed bipolar process and a new and unique architectural design. The AD8012 basically uses a two gain stage complementary design approach versus the traditional "single stage" complementary mirror structure sometimes referred to as the Nelson amplifier. Though twin stages have been tried before, they typically consumed high power since they were of a folded cascade design much like the AD9617. This design allows for the standing or quiescent current to add to the high signal or slew current-induced stages. In the time domain, the large signal output rise/fall time and slew rate is typically controlled by the small signal BW of the amplifier and the input signal step amplitude respectively, not the dc quiescent current of the gain stages (with the exception of input level shift diodes Q1/Q2). Using two stages vs. one also allows for a higher overall gain bandwidth product (GBWP) for the same power, thus lower signal distortion and the ability to drive heavier external loads. In addition, the second gain stage also isolates (divides down) A3's input reflected load drive and the nonlinearities created resulting in relatively lower distortion and higher open-loop gain.

Overall, when "high" external load drive and low ac distortion is a requirement, a twin gain stage integrating amplifier like the AD8012 will provide excellent results for lower power over the traditional single stage complementary devices. In addition, being a CF amplifier, closed-loop BW variations versus external gain variations (varying RN) will be much lower compared to a VF op amp, where the BW varies inversely with gain. Another key attribute of this amplifier is its ability to run on a single 5 V supply due in part to its wide common-mode input and output voltage range capability. For 5 V supply operation, the device obviously consumes half the quiescent power (vs. 10 V supply) with little degradation in its ac and dc performance characteristics. See data sheet comparisons.

DC GAIN CHARACTERISTICS

Gain stages A1/A1B and A2/A2B combined provide negative feedforward transresistance gain. See Figure 40. Stage A3 is a unity gain buffer which provides external load isolation to A2. Each stage uses a symmetrical complementary design. (A3 is also complementary though not explicitly shown). This is done to reduce both second order signal distortion and overall quiescent power as discussed above. In the quasi dc to low frequency region, the closed loop gain relationship can be approximated as:

$G = 1+R_F/R_N$ noninverting operation

$G = -R_F/R_N$ inverting operation

These basic relationships above are common to all traditional operational amplifiers.

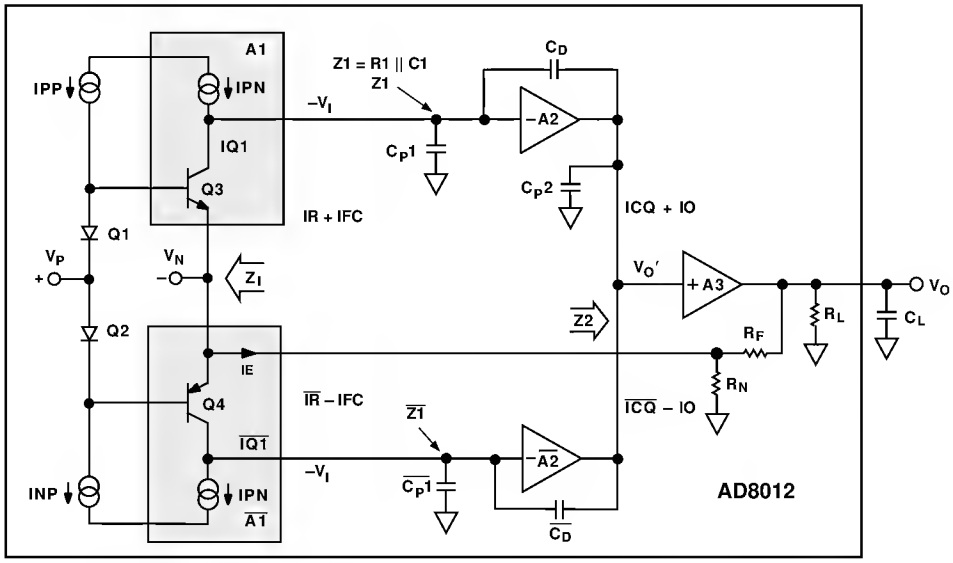


Figure 40. Simplified Block Diagram

APPLICATIONS

Line Driving for HDSL

High Bitrate Digital Subscriber Line (HDSL) is becoming popular as a means of providing full duplex data communication at rates up to 1.544 MBPS or 2.048 MBPS over moderate distances via conventional telephone twisted pair wires. Traditional T1 (E1 in Europe) requires repeaters every 3,000 feet to 6,000 feet to boost the signal strength and allow transmission over distances of up to 12,000 feet. In order to achieve repeaterless transmission over this distance, an HDSL modem requires transmitted power level of +13.5 dBm (assuming a line impedance of 135 Ω).

HDSL uses the Two Binary/One Quaternary line code (2B1Q). A sample 2B1Q waveform is shown in Figure 41. The digital bit stream is broken up into groups of two bits. Four analogue voltages (called quaternary symbols) are used to represent the four possible combinations of two bits. These symbols are assigned arbitrary names +3, +1, –1 and –3. The corresponding voltage levels are produced by a DAC that is usually part of an Analog Front End Circuit (AFEC). Before being applied to the line, the DAC output is low-pass filtered and acquires the sinusoidal form shown in Figure 41. Finally, the filtered signal is applied to the line driver. The line voltages that correspond to the quaternary symbols +3, +1, –1 and –3 are 2.64 V, 0.88 V, –0.88 V and –2.64 V. This gives a peak-to-peak line voltage of 5.28 V.

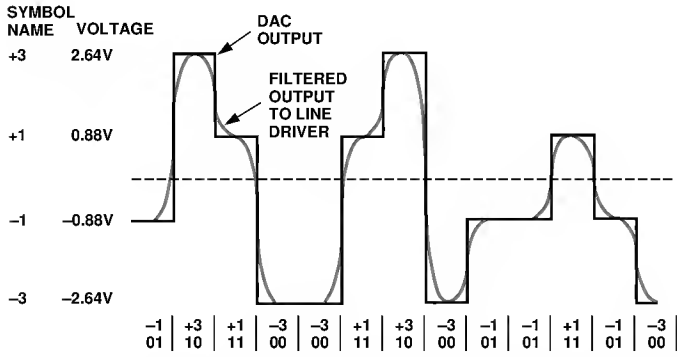


Figure 41. Time Domain Representation of a HDSL Signal

Many of the elements of a classic differential line driver are shown in the HDSL line driver in Figure 42. A 6 V peak-to-peak differential signal is applied to the input. The differential gain of the amplifier ($1+2\ R_F/R_G$) is set to +2, so the resulting differential output signal is 12 V p-p.

As is normal in telephony applications, a transformer galvanically isolates the differential amplifier from the line. In this case a 1:1 turns ratio is used. In order to correctly terminate the line, it is necessary to set the output impedance of the amplifier to be equal to the impedance of the line being driven (135 Ω in this case). Because the transformer has a turns ratio of 1:1, the impedance reflected from the line is equal to the line impedance of 135 Ω ($R_{REFL} = R_{LINE}/\text{Turns Ratio}^2$). As a result, two 66.5 Ω resistors correctly terminate the line.

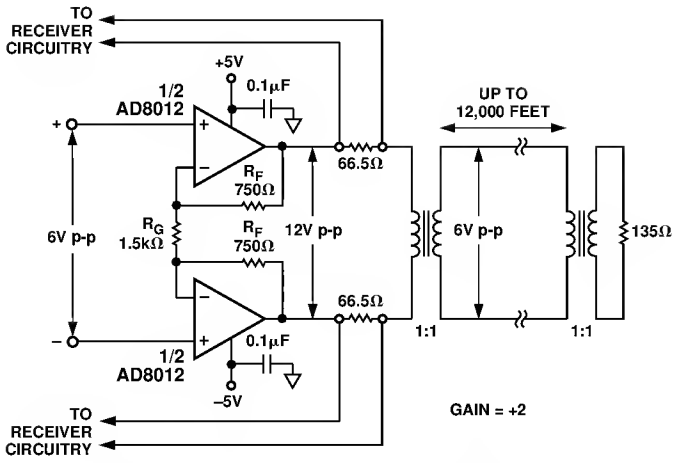


Figure 42. Differential for HDSL Applications

The immediate effect of back-termination is that the signal from the amplifier is halved before being applied to the line. This doubles the power the amplifier must deliver. However, the back-termination resistors also play an important second role.

Full-duplex data transmission systems like HDSL simultaneously transmit data in both directions. As a result, the signal on the line and across the back termination resistors is the composite of the transmitted and received signal. The termination resistors are used to tap off this signal and feed it to the receive circuitry. Because the receive circuitry "knows" what is being transmitted, the transmitted data can be subtracted from the digitized composite signal to reveal the received data.

Driving a line with a differential signal offers a number of advantages compared to a single-ended drive. Because the two outputs are always 180 degrees out of phase relative to one another, the differential signal output is double the output amplitude of either of the op amps. As a result, the differential amplifier can have a peak-to-peak swing of 16 V (each op amp can swing to ±4 V), even though the power supply is ±5 V.

In addition to this, even-order harmonics (2nd, 4th, 6th, etc.) of the two single-ended outputs tend to cancel out one another, so the Total Harmonic Distortion (quadratic sum of all harmonics) decreases compared to the single-ended case, even as the signal amplitude is doubled. This is particularly advantageous for the case of the second harmonic. As it is very close to the fundamental, filtering becomes difficult. In this application, the THD is dominated by the third harmonic which is 65 dB below the carrier (i.e., Spurious Free Dynamic Range = –65 dBc).

Differential line driving also helps to preserve the integrity of the transmitted signal in the presence of Electro-Magnetic Interference (EMI). EMI tends to induce itself equally on to both the positive and negative signal line. As a result, a receiver with good common-mode rejection, will amplify the original signal while rejecting induced (common-mode) EMI.

Choosing the Appropriate Turns Ratio for the Transformer
Increasing the peak-to-peak output signal from the amplifier in the previous example, combined with a variation in the turns ratio of the transformer, can yield further enhancements to the circuit. The output signal swing of the AD8012 can be increased to about ±3.9 V before clipping occurs. This increases the peak-to-peak output of the differential amplifier to 15.6 V. Because the signal applied to the primary winding is now bigger, the transformer turns ratio of 1:1 can be replaced with a (step-down) turns ratio of about 1.3:1 (from amplifier to line). This steps the 7.8 V peak-to-peak primary voltage down to 6 V. This is the same secondary voltage as before so the resulting power delivered to the line is the same.

The received signal, which is small relative to the transmitted signal, will, however be stepped up by a factor of 1.3. Amplifying the received signal in this manner enhances its signal-to-noise ratio and is useful when the received signal is small compared to the to-be-transmitted signal.

The impedance reflected from the 135 Ω line now becomes 228 Ω (1.3^2 times 135 Ω). With a correctly terminated line, the amplifier must now drive a total load of 456 Ω (114 Ω + 114 Ω + 228 Ω), considerably less than the original 270 Ω load. This reduces the drive current from the op amps by about 40%.

More significant however is the reduction in dynamic power consumption; that is, the power the amplifier must consume in order to deliver the load power. Increasing the output signal so that it is as close as possible to the power rails, minimizes the power consumed in the amplifier.

There is, however, a price to pay in terms of increased signal distortion. Increasing the output signal of each op amp from the original ±3 V to ±3.9 V reduces the Spurious Free Dynamic Range (SFDR) from –65 dB to –50 dB (measured at 500 kHz), even though the overall load impedance has increased from 270 Ω to 456 Ω.

LAYOUT CONSIDERATIONS

The specified high speed performance of the AD8012 requires careful attention to board layout and component selection. Table I shows recommended component values for the AD8012 and Figures 44–49 show recommended layouts for the 8-lead SOIC and microSOIC packages for a positive gain. Proper RF design techniques and low parasitic component selections are mandatory.

The PCB should have a ground plane covering all unused portions of the component side of the board to provide a low impedance ground path. The ground plane should be removed from the area near the input pins to reduce stray capacitance.

Chip capacitors should be used for supply bypassing (see Figure 43). One end should be connected to the ground plane and the other within 1/8 in. of each power pin. An additional (4.7 μF–10 μF) tantalum electrolytic capacitor should be connected in parallel.

The feedback resistor should be located close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance greater than 1.5 pF at the inverting input will significantly affect high speed performance when operating at low noninverting gains.

Stripline design techniques should be used for long signal traces (greater than about 1 in.). These should be designed with the proper system characteristic impedance and be properly terminated at each end.

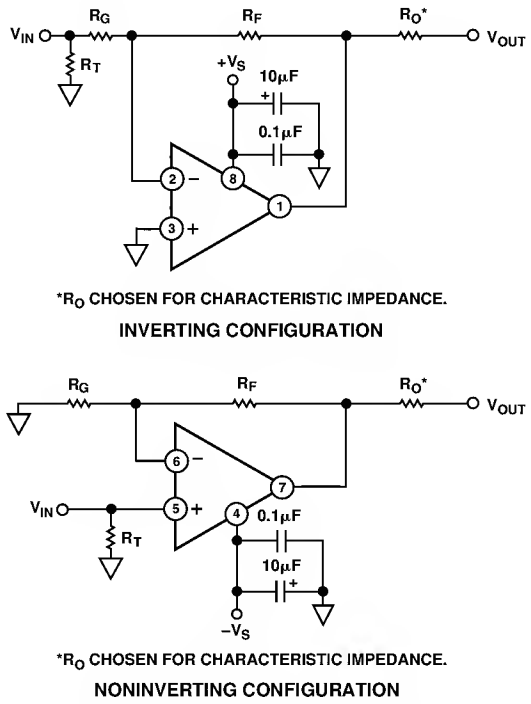


Figure 43. Inverting and Noninverting Configurations

Table I. Typical Bandwidth vs. Gain Setting Resistors

Gain	R_F	R_G	R_T	Small Signal –3 dB BW (MHz), V_S = ±5 V, R_L = 1 kΩ
–1	750 Ω	750 Ω	53.6 Ω	110
+1	750 Ω	–	49.9 Ω	350
+2	750 Ω	750 Ω	49.9 Ω	150
+10	750 Ω	82.5 Ω	49.9 Ω	40

R_T chosen for 50 Ω characteristic input impedance.

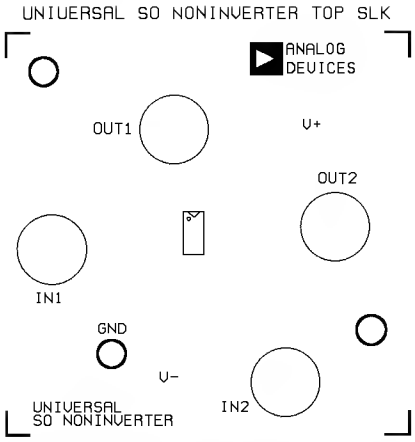


Figure 44. Universal SOIC Noninverter Top Silkscreen

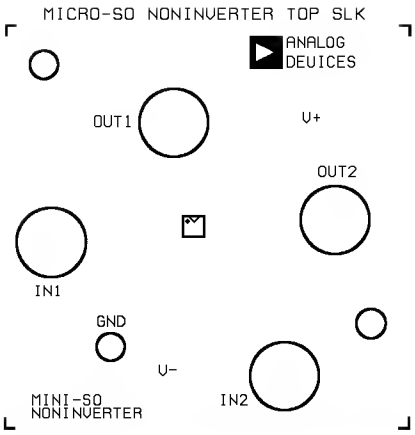


Figure 47. Universal microSOIC Noninverter Top Silkscreen

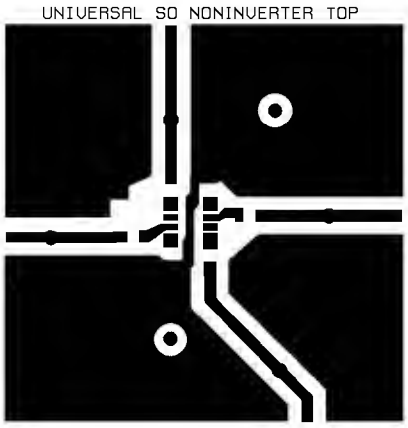


Figure 45. Universal SOIC Noninverter Top

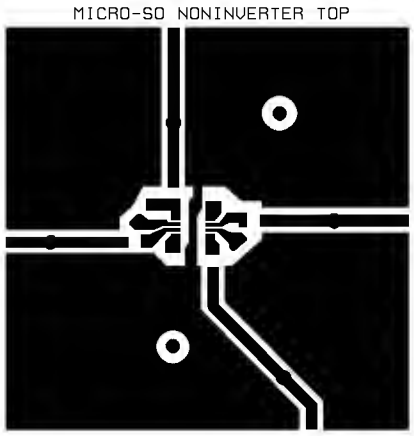


Figure 48. Universal microSOIC Noninverter Top

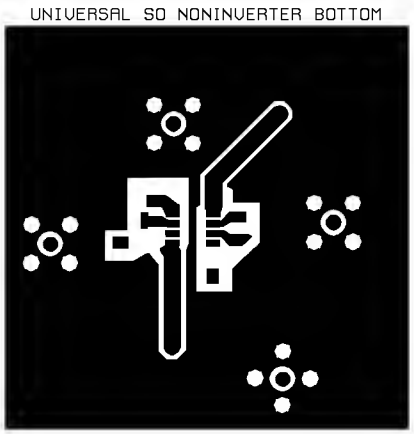


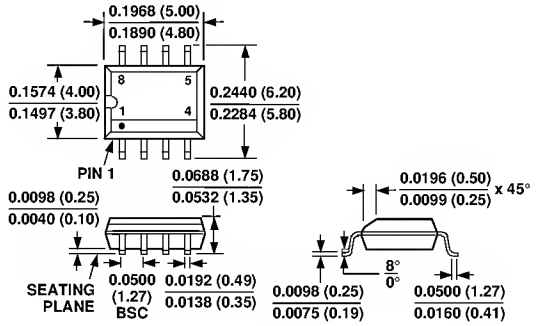
Figure 46. Universal SOIC Noninverter Bottom

Figure 49. Universal microSOIC Noninverter Bottom

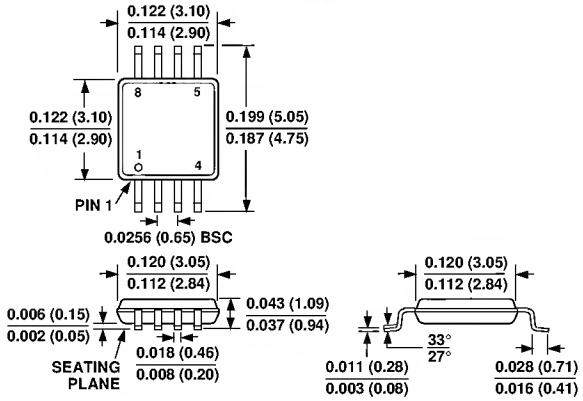
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC (SO-8)



8-Lead microSOIC (RM-08)



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